South Asian Journal of Research in Engineering Science and Technology

www.sajrest.com

SAJREST©2018 e-ISSN: 2455-9261

Volume 3, Issue **11**, **November 2018**

pp. **34--38**

PERFORMANCE ANALYSIS OF MULTIPLE VALUED GATES

S.Praveenkumar [1], S.Jim Hawkinson [2], M.Vijayakumar [3]
PG Scholar, [1], Asst. Professor,[2], Asso. Professor[3],
ECE Department,
E.G.S Pillay Engineering College,
Nagapattinam

***Abstract*:** Interconnections are increasingly the dominant contributor to delay, area and energy consumption in CMOS digital circuits. Multiple-valued logic can decrease the average power required for level transitions and reduces the number of required interconnections, hence also reducing the impact of interconnections on overall energy consumption. The design of Multiple Valued Logic (MVL) digital circuits is performed by increasing the representation domain from the two level (N=2) switching algebra to N > 2 levels. Universal sets of MVL CMOS gates allow the synthesis and implementation of any MVL digital circuit. The MVL operators are eAND1, eAND2, eAND3, Successor (SUC), and Maximum (MAX). These operators are used to perform synthesis of any MVL digital circuits.

Keywords---CMOS,digitalcircuits,multivaluedlogic

I. INTRODUCTION

Presently all the digital circuit synthesis is done in two level logic (N=2), where D = {0, 1} is the domain of numerical representation. Whereas if we increase the domain D = {0, 1, 2… L = N-1}, the synthesis of multi valued logic circuit is possible. MVL is also known as many valued or multiple valued or multi valued which traces its origin from the Post algebra and Lukasiewicz logic [1], [2].

First basic ideas on MVL come from ternary MVL proposed by Lukasiewicz in his logic. He claimed that the three-valued (ternary) logic is as consistent and free of contradictions as the two-valued logic. Three-valued logic is utilized to design ternary circuits with domain either with G= [0, 1, 2] or balanced ternary with G = [-1, 0, 1]. In a ternary Post algebra, the literal, the AND, and the OR form.

The current trend in integrated circuit is to embed multiple systems into single IC, known as System on chip leading .

other things, an increment in the quantity of delay time, length and complexity of the inter connection of Advantage of fast development a tool that can develop circuit in multivalued system and convert that in binary system for implementation purpose. Hence proposed tool will have the capabilities:

- ✓ Multivalued circuit schematic creation, editing , and saving.
- ✓ To integrate circuit components.
- ✓ Showing the every gate level property like truth table.
- ✓ Drawing of connectivity of gates.
- ✓ Binary conversion testing and binary converted circuit.

II. MVL PRINCIPLES

Multiple Value Logic function will represent the value in domain D = {0, 1, …., N = L-1} and then a unique truth table can be obtained. Analogous to Products of Sums (POS) or Sum of Products (SOP) which is a unique representation of the function for binary algebra , canonical Sum of Extended Products (SOEP) form is defined for universal set of operators for quaternary MVL algebra. The already mentioned operators SUC, MAX, eAND1, eAND2, eAND3 in the introduction, define a universal set for quaternary logic under the proposed algebra.

the complete set of operations, and also, the literal and the NAND operations form a complete set. In ternary for the proposed algebra the universal set is eAND1, eAND2, SUC, MAX. Ternary and quaternary circuits have been studied increasingly in recent years.

Quaternary circuits have the practical advantage that a four-valued signal can easily be transformed into a two-valued signal. Then, to define an algebra, convenient to use and easy to learn, with a well-known methodology, feasible to implement from the algorithmic (minimization tools) and gates (IC CMOS hardware) point of views, a suitable criteria is to extend well known concepts of the binary switching algebra.

As we feel that development in multivalued logic is comparatively, easier, faster and better understandable and likely to become new development environment but devices capable of implementing this logic have not yet become available.

III. MVL ALGEBRA

The Multiple Valued Logic algebra is an ordered set with domain D = [0, 1, 2, 3… N-1] in which acting two binary operators(Maximum and Extended AND, respectively) and Successor as defined below, with the lower element 0 and the upper element (N-1).

I. ***Definition 1:****INVERTER*

TABLE-I

Input(x)	Output(y)
0	3
1	2
2	1
3	0

The output signal expression or the complement function is calculated as:

$y = r - 1 - X$

Here, r = radix of the system,

X = input

y = output

***Definition 2*:** Extended AND (e-AND) operator is denoted by x*^constant y=x=y=constant otherwise output is 0

For ex
X*^1 y x=y=1 otherwise =0
There are three type of and operators

I. Extended AND 1 operators
II. Extended AND 2 operators
III. Extended AND 3. Operators

TABLE-II TRUTH TABLE

X=INPUT	Y=INPUT	Z=OUTPUT
0	0	0
0	1	0
0	2	0
0	3	0
1	0	0
1	1	**1**
1	2	0
1	3	0
2	0	0
2	1	0
2	2	**2**
2	3	0
3	0	0
3	1	0
3	2	0
3	3	**3**

***Definition 3*:** Max operator

MAX OPERATOR =X+Y
X≥Y=X
X≤Y=Y

TABLE-III TRUTH TABLE

X=INPUT	Y=INPUT	Z=OUTPUT
0	0	0
0	1	1
0	2	2
0	3	3
1	0	1
1	1	1
1	2	2
1	3	3
2	0	2
2	1	2
2	2	2
2	3	3
3	0	3
3	1	3
3	2	3
3	3	3

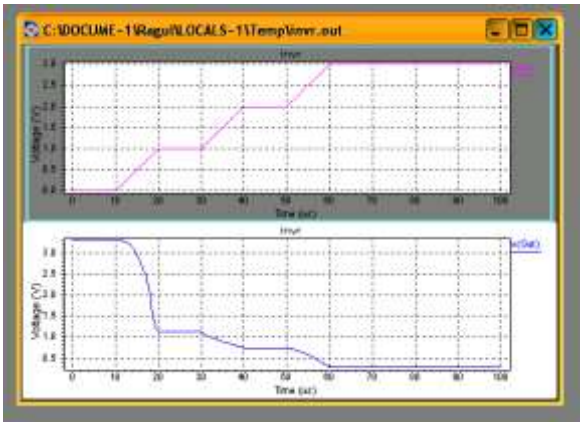
TABLE-IV MVL POSTULATES

Identify for +: a1+0= a1; 0+ a1= a1
Associativity of +, *i: a1+ (a2+ a3)= (a1+ a2)+ a3 a1*i (a2*i a3)= (a1*i a2)*i a3
Commutativelyof +,*i a1+a2=a2+a1 a1*i a2=a2*ia1
Complement for +,*i a10|a11|a12|…. |a1 (N-1)=(N-1); a10*i a11*i a12*i …. *i a1 (N-1)=0;
Idempotency of + a1+a1=a1

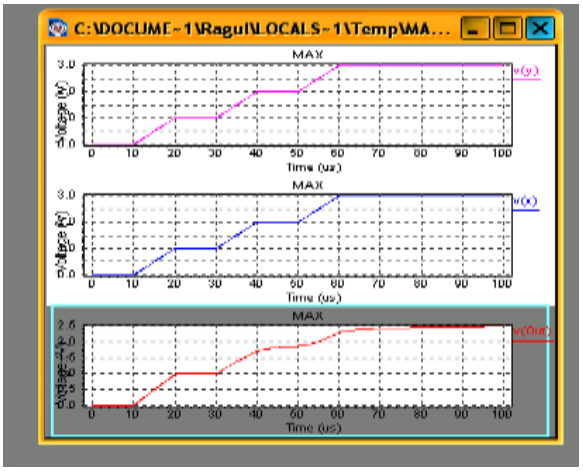
IV. SYNTHESIS OF MVL CIRCUITS

The Quaternary inverter circuit is an essential function various logic circuits. Function of inverter is to just complement the input signal. The logic level “0”, logic level “1”, logic level “2” and logic level “3” are represented by voltages 0V, 1V, 2V and 3V respectively in 250nm CMOS technology.

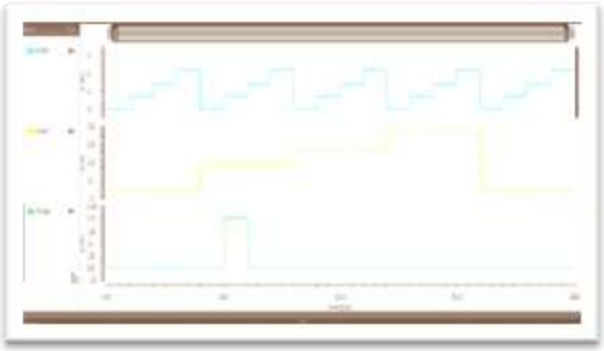
A. SIMULATION RESULT OF QUATERNARY INVERTER



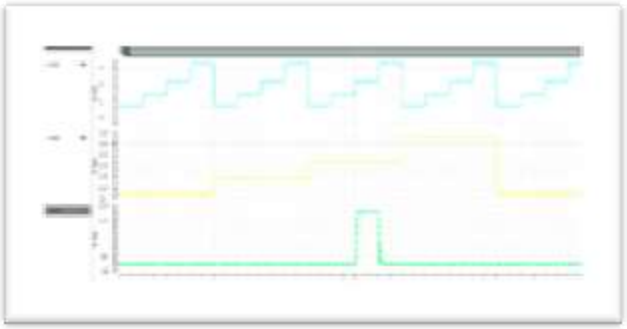
B. SIMULATION RESULT OF MAX GATE



C. SIMULATION RESULT OF QUATERNARY EXTENDED AND1 GATE



D. SIMULATION RESULT OF QUATERNARY EXTENDED AND 2 GATE



E. SIMULATION RESULT OF QUATERNARY EXTENDED AND 3 GATE

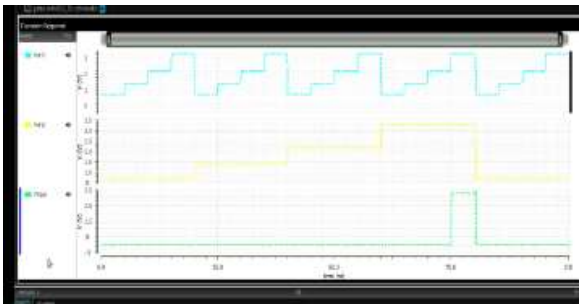


TABLE-V
POWER CONSUMPTION

CMOS GATE	POWER CONSUMPTION		
	BINARY	TERNARY	QUATENARY
Inverter	0.1nw	0.2nw	27.1pw
Max	67.1uw	0.68nw	0.4uw
E-and-1	38.9uw	0.5mw	2.1uw
E-and-2	37.9uw	0.4mw	2.0uw
E-and-3	36.1uw	0.4mw	1.1uw

V. CONCLUSION

This paper present implementation of quaternary basic logic cells such as inverter, NAND and NOR. CMOS technology is used to design the logic cells. The circuits are simulated using TANNER SPICE.
Circuit complexity has been reduced by using three values of enhancement mode threshold voltage and by utilizing a priority rule in establishing the output voltage i.e. the priority is given to low level at all times when several transistors are in the ON state. This principle of operation leads to the marked decrease in the in the transistor number and exact transient response.

VI. FUTURE WORK

Quaternary logic cells are designed using SPICE low-level model parameters. In future, the work could be extended to higher level model parameters. This work can further be extended by layout extraction from SPICE code of the logic cells. The layout can further be optimized to get results nearer to ideal conditions

REFERENCE

[1] Universal Set of CMOS Gates for the Synthesis of Multiple Valued Logic Digital Circuits.
IEEE transactions on circuits and systems—i: regular papers, vol. 61, no. 3, march 2014
Milton Ernesto Romero, Evandro Mazina Martins, Ricardo Ribeiro dos Santos, and Mario Enrique Duarte Gonzalez.

[2] Miller, D.M. Thornton, and M.A. ―Multiple Valued Logic: Concepts and Representations‖,Synthesis Lectures on Digital Circuits and Systems, Morgan & Claypool Publishers, 2007.

[3] Smith, K.C., ―The Prospects for Multivalued Logic- A Technology and Applications View‖,Computers, IEEE Transactions on, 30, pp. 619-634, 1981.

[4] Fijany, A., Vatan, F.Mojarradi, M., Toomarian, B. Blalock, B.Akarvardar, K. Cristoloveanu,S. and Gentil, P. ―The G4-FET- a universal and programmable logic gate‖, Proceedings of the 15th ACM Great Lakes symposium on VLSI (GLSVLSI2005), pp. 349-352, April 2005.

[5] Vasundara Patel K S, and K S Gurumurthy, ―Quaternary Sequential Circuits‖ IJCSNSInternational Journal of Computer Science and Network Security, VOL.10 No.7, July 2010.

[6] Vasundara Patel k s, and k s gurumurthy; ―Arithmetic operation in multivalued logic
―International journal of vlsi design & communication system (VLSCS) , vol 1, no 1, march2010.

[7] Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi, ―Design of a Ternary Memory Cell Using CNTFETs‖ IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 11, NO. SEPTEMBER 2012.

[8]S.Jim Hawkinson,"Analysis and Performance comparison of CMOS and FinFET for VLSI Applications", IJETAE, volume 3 , issue 2, Feb 2013.